Boost Regulator for Display Bias or LED Driver

Not for New Design

These parts are in production but have been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available.

Date of status change: November 1, 2008

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

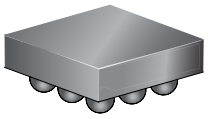
Boost Regulator for Display Bias or LED Driver

Features and Benefits

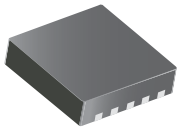
- Output disconnect during shutdown
  - 1 µA shutdown current
- 2.7 to 9 V input
  - Operate with 1 or 2 Li+ battery input supply
- Output voltage up to 23 V
- 1.2 MHz switching frequency
- 1.5 A switch current limit
- Internal overvoltage and overtemperature protection, and soft start

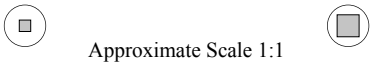
Package:

9-pin CSP (suffix CG)



10-pin MLP/DFN (suffix EJ) with exposed thermal pad





Approximate Scale 1:1

Description

The A8480 is a 1.2 MHz optimized boost converter with internal soft-start and compensation to support WLED, flash/torch, and display bias applications. The input voltage range of 2.7 to 9 V supports either 1 or 2 Li-ion battery applications. The high voltage integrated double-diffused MOSFET (DMOS) allows output voltages as high as 23 V with a switch current limit of 1.5 A, this increases the maximum quantity of LEDs that can be used in series.

To maximize battery life in the application, the output can be completely disconnected from the battery voltage to virtually eliminate leakage current in the system. The disconnect switch can pass up to 80 mA current. For system protection, the A8480 has internal overtemperature and overvoltage protection.

The A8480 can be used as a general purpose boost converter by taking power through the CAP pin. In this configuration, it can provide up to 520 mA at 12 V with 5.5 V input voltage.

The A8480 is available in both 1.6 mm × 1.6 mm, 0.5 mm nominal height CSP, and 3 mm × 3 mm, 0.75 mm nominal height MLP/DFN packages.

Applications include:

- WLED flash/torch
- WLED backlight
- OLED bias supplies
- LCD bias supplies
- General purpose boost converter

Typical Applications

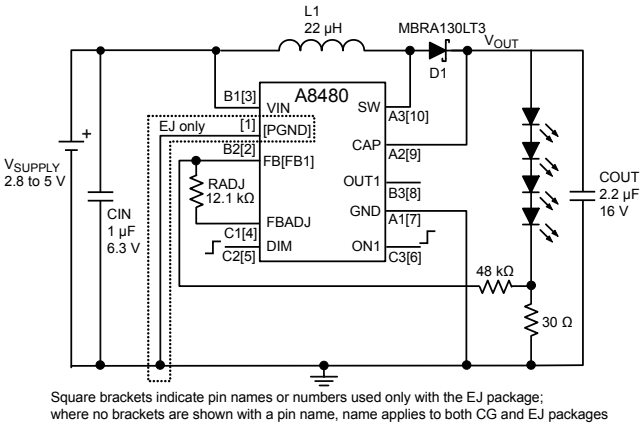


Figure 1. Using the A8480 to drive a flash (100 mA) or torch (20 mA)

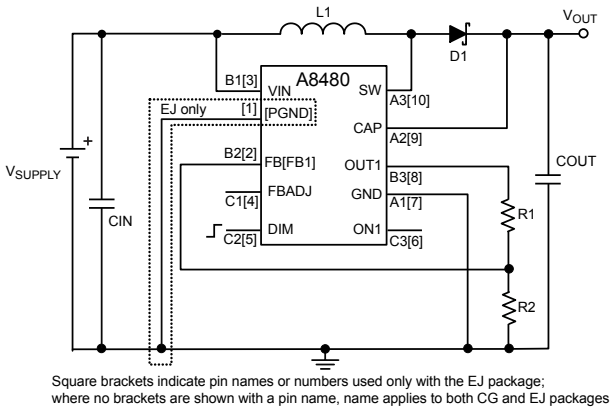
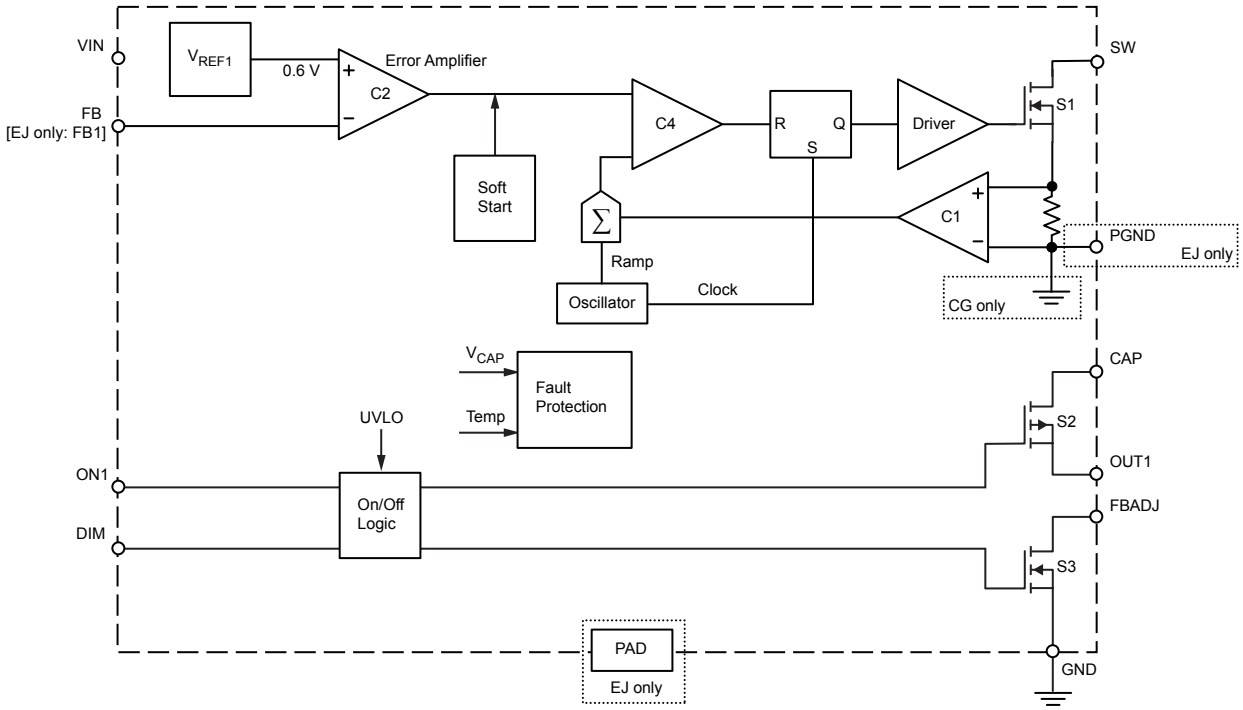


Figure 2. The A8480 used as a general boost

Functional Block Diagram



Absolute Maximum Ratings

Input or Output Voltage

SW, CAP, OUT1, FBADJ pins ..... **–0.3 to 26 V**

VIN pin, V_{IN} ..... **–0.3 to 9.5 V**

All other pins, V_x ..... **–0.3 to V_{IN} + 0.3 V (7 V max.)**

Operating Ambient Temperature, T_A ..... **–40°C to 85°C**

Maximum Junction Temperature, T_J(max) ..... **150°C**

Storage Temperature, T_{stg} ..... **–55°C to 150°C**

Package Thermal Characteristics

CG package: 109 °C/W, on a 2-sided board. Please refer to page 14 for test board layout.

EJ package: $R_{\theta JA}$ = 45 °C/W, on a 4-layer board.

Additional information is available on the Allegro Web site.

Packages are lead (Pb) free.

EJ package has 100% matte tin leadframe plating.

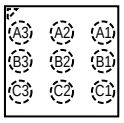
Selection Guide

Part Number	Package	Packing[a]
A8480ECGLT-T[b]	9-bump chip scale package	Tape and Reel
A8480EEJTR-T	10-pin MLP/DFN package	1500 pieces per reel

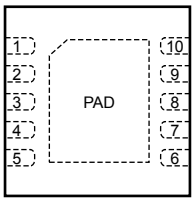
[a]Contact Allegro for additional packing options.

[b]Contact Allegro factory for availability.

Pin-out Diagrams



CG Package
(Top View)



EJ Package
(Top View)

Terminal List Table

Number		Name	Description
CG	EJ		
–	1	PGND	Power ground connection; use to avoid interference with signal ground.
A1	–	GND	Power and signal ground connection; connect directly to the ground plane.
–	7	GND	Signal ground reference; connect directly to the ground plane.
A2	9	CAP	This is the connection to the output capacitor for the boost regulator output.
A3	10	SW	This is the connection between the internal boost switch and the external inductor. Because rapid changes of current occur at this pin, the board traces connected to this pin should be minimized and the inductor and diode should be connected as close to this pin as possible.
B1	3	VIN	This is the power input supply connection to the circuit. A bypass capacitor tying this pin to GND must be connected close to this pin.
B2	–	FB	This is the feedback pin for controlling voltage on the OUT1 pin. The nominal reference voltage on this pin is 600 mV. In order to minimize noise, connect the feedback resistor network close to this pin.
–	2	FB1	
B3	8	OUT1	This is the voltage-controlled output pin for the OLED drive. An internal switch disconnects the OLED during shutdown.
C1	4	FBADJ	Open collector output driven by DIM. This can be used to provide dimming by connecting an additional feedback circuit or it can be used to drive external output.
C2	5	DIM	Logic input. Driving DIM puts the FBADJ open collector output low.
C3	6	ON1	This is the enable pin for OUT1.
–	PAD	–	Exposed thermal pad. Connect to GND plane for enhanced thermal performance.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, VIN = ON1 = DIM = 3.0 V (unless noted otherwise)

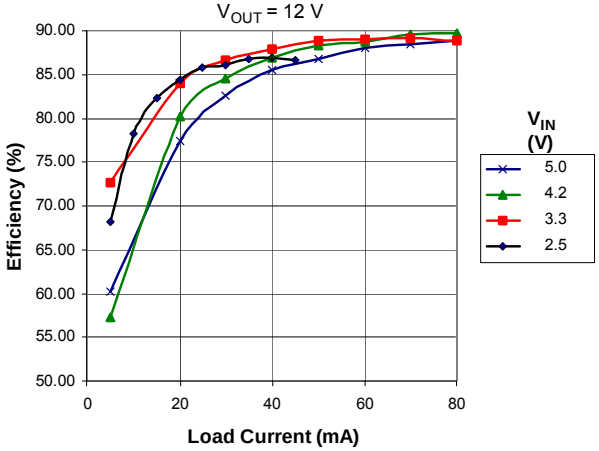
Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Voltage Range	V_{IN}		2.7	–	9	V
Quiescent Input Current	$I_{IN(Q)}$	DIM=ON1=0	–	–	1	µA
Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} rising	2.25	2.45	2.60	V
Feedback Reference Voltage	V_{FB}		584	610	636	mV
Feedback Voltage Line Regulation		2.7 V ≤ V_{IN} ≤ 9 V	–	0.1	–	%/V
Feedback Input Current	I_{FB}		–	45	100	nA
Switch Current Limit	I_{SWLim}		–	1.5	–	A
Switch Frequency	f_{SW}		1	1.2	1.4	MHz
Switch Maximum Duty Cycle*	DC		85	90	–	%
Switch S1 On Resistance	$R_{DS(on)1}$	I_{SW} = 0.5 A	–	225	–	mΩ
Switch S2 On Resistance	$R_{DS(on)2}$	I_{SW} = 80 mA	–	3.5	–	Ω
Switch S1 Leakage Current	$I_{SW(lkg)1}$	V_{SW} = 5 V	–	–	1	µA
Switch S2 Leakage Current	$I_{SW(lkg)2}$		–	–	1	µA
FBADJ MOSFET On Resistance	$R_{DSF(on)}$	V_{DIM} > V_{IH}	–	10	–	Ω
FBADJ MOSFET Leakage Current	$I_{FBADJ(lkg)}$	V_{DIM} < V_{IL}, V_{FBADJ} = 0.6 V	–	1	–	µA
ON1, DIM Input Threshold Low	V_{IL}		–	–	0.4	V
ON1, DIM Input Threshold High	V_{IH}		1.5	–	–	V
ON1, DIM Input Bias Current	I_{IB}		–	65	–	µA
Output Overvoltage Rising Limit	V_{OVPR}		–	24.5	25.5	V
Thermal Shutdown Threshold	T_{SHDN}		–	160	–	°C
Thermal Shutdown Hysteresis	$T_{SHDNhys}$		–	10	–	°C
Soft-Start Period	t_{SS}	V_{OUT} = 10 V	–	2	–	ms

*Guaranteed by design.

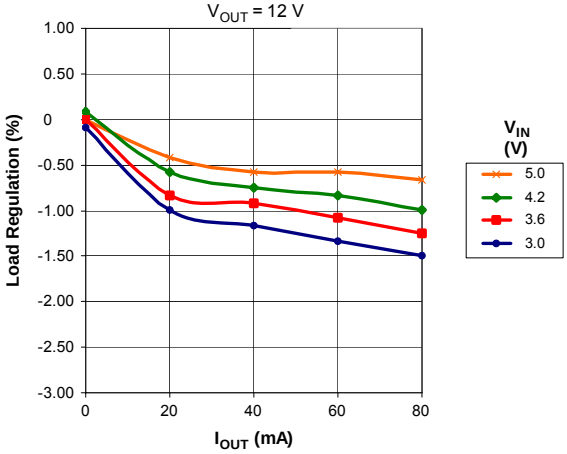
Performance Characteristics

Tests performed using application circuit shown in figure 5
L1 = 4.7 µH, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C (unless otherwise noted)

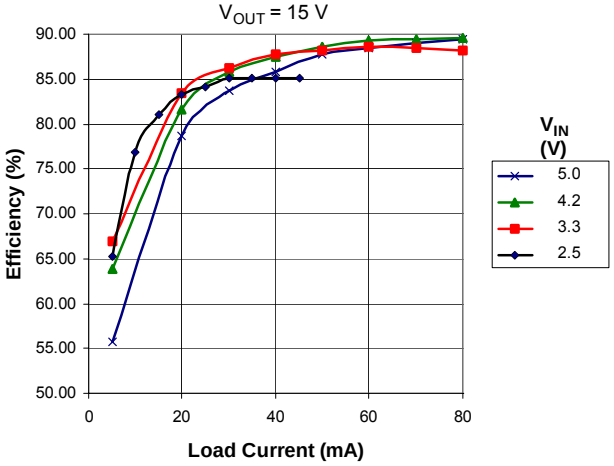
Efficiency versus Load Current
V_{OUT} = 12 V



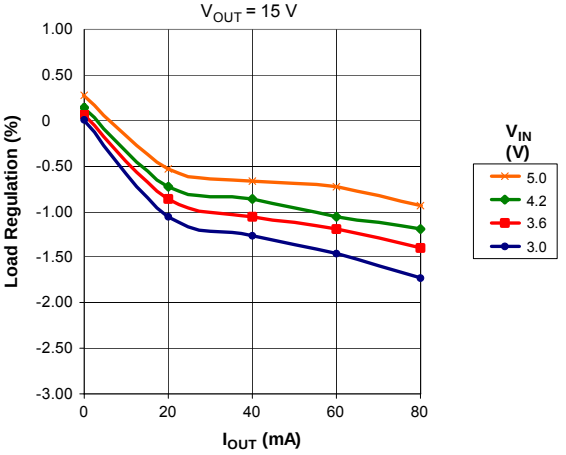
Load Regulation
V_{OUT} = 12 V



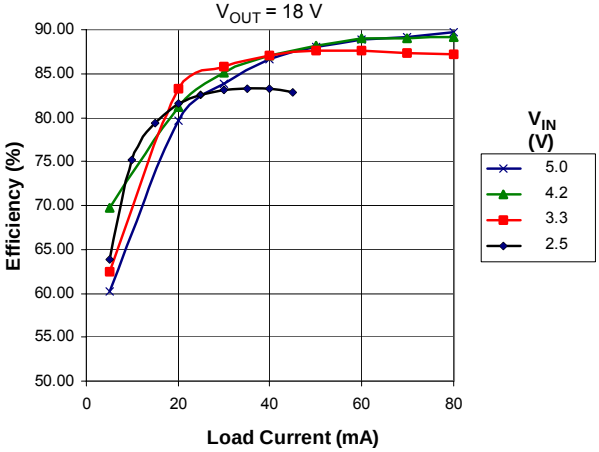
Efficiency versus Load Current
V_{OUT} = 15 V



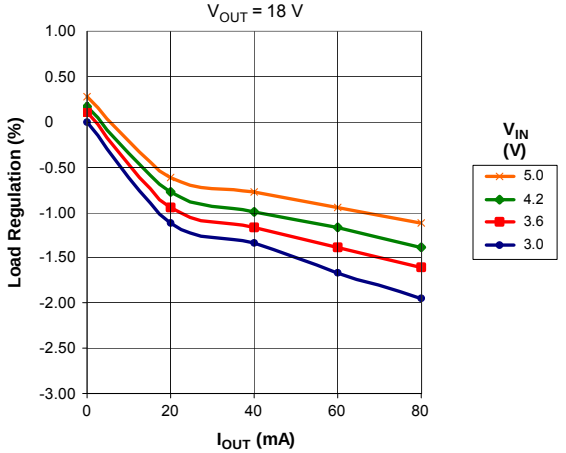
Load Regulation
V_{OUT} = 15 V



Efficiency versus Load Current
V_{OUT} = 18 V



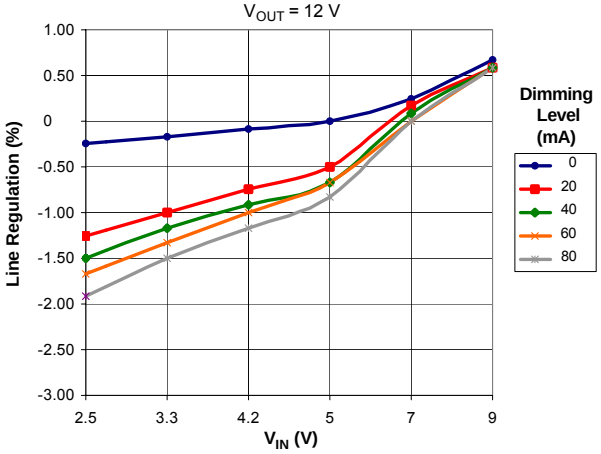
Load Regulation
V_{OUT} = 18 V



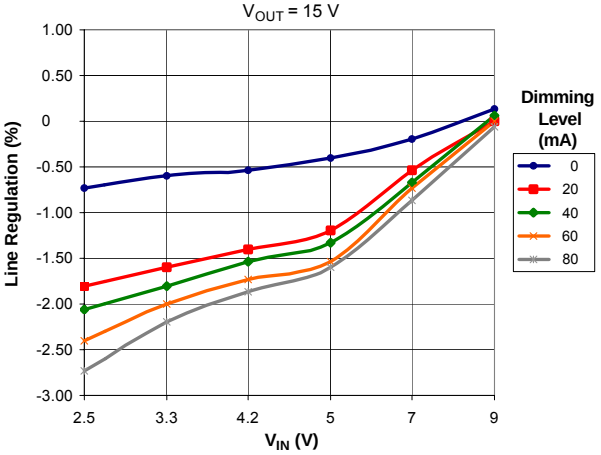
Performance Characteristics

Tests performed using application circuit shown in figure 5
L1 = 4.7 µH, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C (unless otherwise noted)

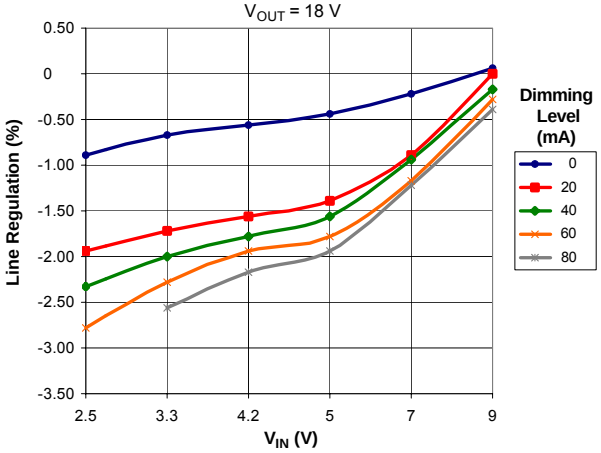
Line Regulation
V_{OUT} = 12 V



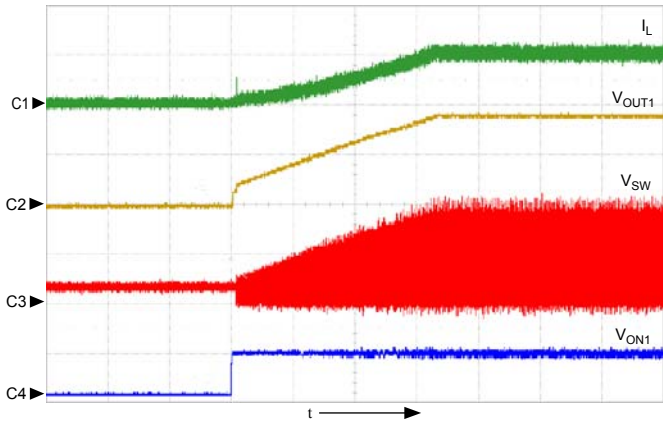
Line Regulation
V_{OUT} = 15 V



Line Regulation
V_{OUT} = 18 V

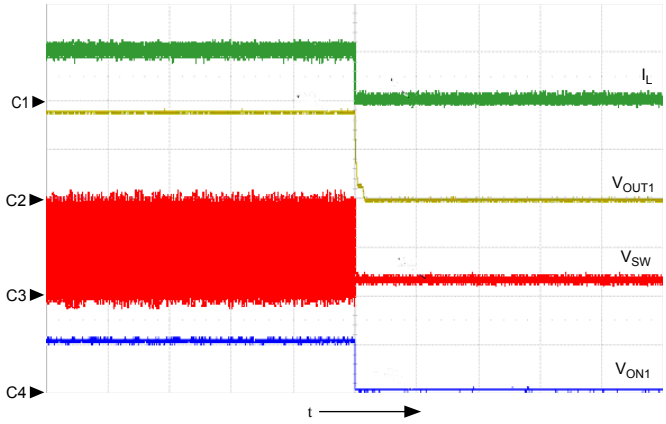


Startup



Symbol	Parameter	Units/Division
C1	I_L	500 mA
C2	V_{OUT1}	10.0 V
C3	V_{SW}	10.0 V
C4	V_{ON1}	2.00 V
t	time	1 ms
Conditions	**Parameter**	**Value**
	V_{IN}	3.3 V
	V_{OUT}	18 V
	I_{OUT}	80 mA

Shutdown

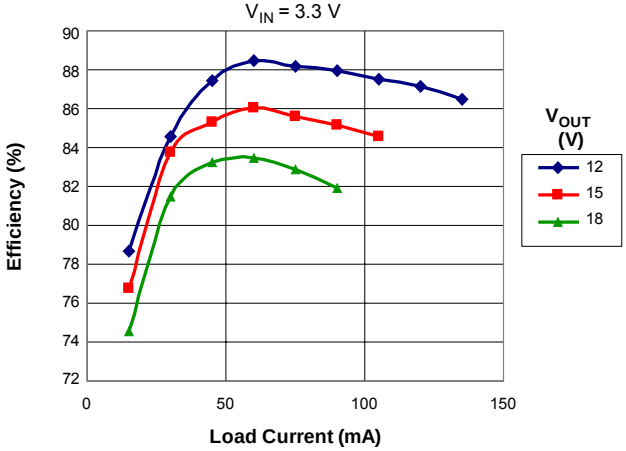


Symbol	Parameter	Units/Division
C1	I_L	500 mA
C2	V_{OUT1}	10.0 V
C3	V_{SW}	10.0 V
C4	V_{ON1}	2.00 V
t	time	5 ms
Conditions	**Parameter**	**Value**
	V_{IN}	3.3 V
	V_{OUT}	18 V
	I_{OUT}	80 mA

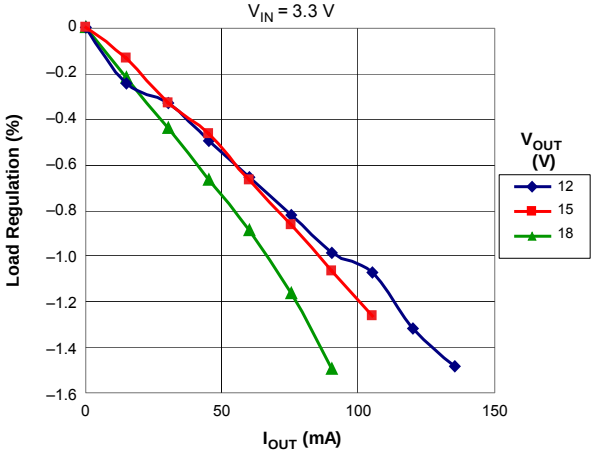
Performance Characteristics

Efficiency and load regulation for general boost without disconnect FET
Tests performed using application circuit shown in figure 2

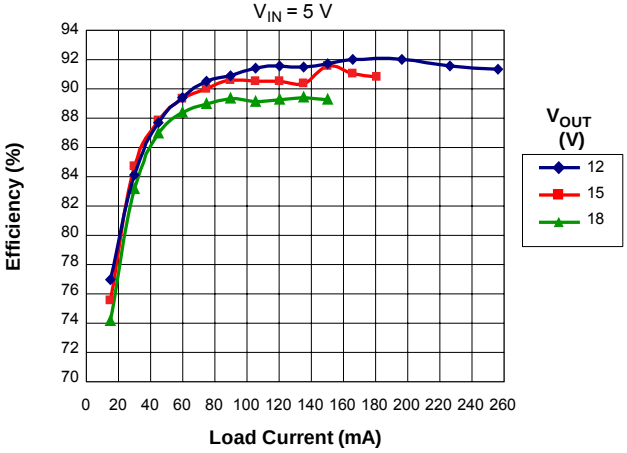
Efficiency versus Load Current
V_{IN} = 3.3 V



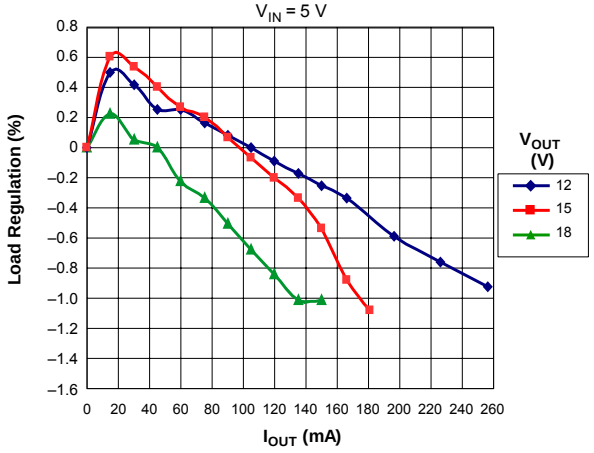
Load Regulation
V_{IN} = 3.3 V



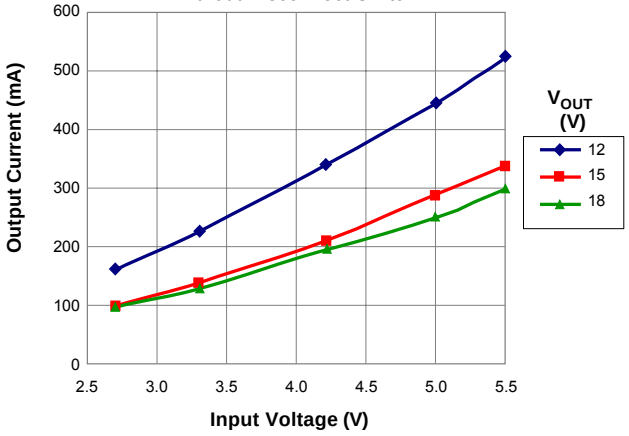
Efficiency versus Load Current
V_{IN} = 5 V



Load Regulation
V_{IN} = 5 V



Maximum Output Current versus Input Voltage
Without Disconnect Switch



Functional Description

The A8480 is a boost converter with output disconnect. The boost stage boosts input battery voltage to a sufficient level to drive an OLED or a set of series-connected WLEDs. This stage uses 1.2 MHz constant frequency, current mode control. Typical application circuits are shown in figure 1, and the Typical Applications section.

When OUT1 is enabled and V_{IN} is greater than V_{IN}(min), the boost stage is ramped-up with soft start, with switch, S2, completely turned on.

The constant voltage drive for OLED is provided through the OUT1 pin. The internal switch between the CAP and OUT1 pins disconnects the OLED when OUT1 is disabled.

For driving OLEDs, output voltage is sensed by the FB1 pin through a voltage divider network. Output voltage (V) is set as:

$$V_{OUT1} = 0.61 \times \frac{R_1 + R_2}{R_2} \quad (1)$$

When DIM is high and RFBADJ is used (R2 is configured in parallel with RFBADJ in the circuit; see figure 5a), the output voltage is set as follows:

$$V_{OUT1} = 0.61 \times \frac{R_1 + \left(\frac{R_2 \times R_{FBADJ}}{R_2 + R_{FBADJ}} \right)}{\frac{R_2 \times R_{FBADJ}}{R_2 + R_{FBADJ}}} \quad (2)$$

The A8480 provides protection against output overvoltage on the CAP pin, overload, and overtemperature. Also, it has an input undervoltage lockout to avoid malfunction and battery drain.

At light loads, instantaneous inductor current drops to zero. This is known as discontinuous mode operation and will result in some low frequency ripple. In discontinuous mode, the voltage at the SW pin will ring, due to the resonant LC circuit formed by the inductor and the switch and diode capacitance. This ringing is low frequency and is not harmful. It can be damped with a resistor across the inductor, but this will reduce efficiency and is not recommended.

Dual OLED Application

The A8480 can be easily used as a dual OLED driver. In this application, the main OLED can be connected to OUT1 and the sub OLED can be connected between the output of the boost stage, at V_{OUT}, and the FBADJ pin, as in the application shown in figure 6. The sub OLED is controlled by the DIM pin. Pulling the DIM pin high turns on the internal switch S3, which pulls the FBADJ pin low, allowing the sub OLED to turn on. Figure 6 shows that the sub OLED is grounded as well.

Applications Information

Component Selection

The component values shown in the application circuits will be sufficient for most applications (typical application circuits are shown in figure 1, and the Typical Applications section). To reduce the output ripple, the output inductor may be increased in value, but in most cases this will result in excessive board area and cost.

Inductor Selection

The inductor is the most important component in the power supply design because it affects the steady-state performance, transient response, and loop stability. The inductance value, DC resistance, and the saturation current should be considered when choosing the inductor. The DC current of the inductor can be calculated by:

$$I_{L\_DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (3)$$

and the inductance value can be calculated by:

$$L_{min} = \frac{V_{imin}}{\Delta_i \times \eta} \times \left(1 - \frac{V_{imin}}{V_{OUT}}\right) \times \frac{1}{f} \quad (4)$$

where Δi = (20% to 40%) × I_{L_DC} is the peak-to-peak ripple current.

Smaller inductance values force the converter into discontinuous mode, which will reduce the maximum output current. Larger inductance values reduce the gain and phase margin, which will result in instability of the loop.

The inductor should have low winding resistance, typically < 0.2 Ω and low 1.2 MHz core loss for better efficiency.

The inductor should have a saturation current higher than 1.5 A, in order to provide 20 V at the OUT1 pin, and 100 mA at 2.7 V_{IN}. For high temperature operation, a suitable derating factor should be considered. Several inductor manufacturers, including: Coilcraft, Murata, Panasonic, Sumida, Taiyo Yuden, and TDK, have and are developing suitable small-size inductors.

Diode Selection

The diode should have a low forward voltage to reduce conduction losses and a low capacitance to reduce switching losses. Schottky diodes can provide both of these features, if carefully selected. The forward voltage drop is a natural advantage for Schottky diodes and decreases as the current rating increases. However, as the current rating increases, the diode capacitance also increases, so the optimum selection is usually the lowest current rating above the circuit maximum.

The diode RMS current rating should be:

$$I_{DIODE(RMS)} = I_{OUT} = I_{IN}\sqrt{1-D} \quad . \quad (5)$$

Diode PIV should be higher than the output voltage on the CAP pin.

Capacitor Selection

The input capacitor selection is based on the input voltage ripple. It can be calculated as:

$$C_{IN}(min) = \frac{\Delta i}{8 \times f_{SW} \times V_{IN(ripple)}} \quad (6)$$

where $V_{IN(ripple)}$ is the input ripple.
The output capacitor selection is based on the output ripple requirement. It can be calculated by:

$$C_{OUT} = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \times \frac{1}{f} \times \frac{I_{OUT}}{V_{ripple(pp)}} \quad (7)$$

where V_{ripple} is the peak-to-peak output ripple.

In addition, the ESR-related output ripple can be calculated by:

$$V_{ripple(ESR)} = I_{OUT} \times ESR \quad . \quad (8)$$

If a ceramic capacitor is selected, the ESR-related ripple can be neglected, due to the low ESR. If a tantalum electrolytic capacitor is selected, this portion of ripple voltage has to be considered.

During load transient response, a larger output capacitance always helps to supply or absorb additional current, which results in lower overshoot and undershoot voltage.

Because the capacitor values are low, ceramic capacitors are the best choice for this application. To reduce performance variation over temperature, low drift types such as X7R and X5R should be used. Recommended specifications are shown in the table below. Suitable capacitors are available from TDK, Taiyo Yuden, Murata, Kemet, and AVX.

The output capacitor is placed on the CAP pin only. An additional capacitor can be added on the OUT1 pin, but it is not needed for proper operation and it cannot replace the capacitor on the CAP pin.

Typical Application Circuits

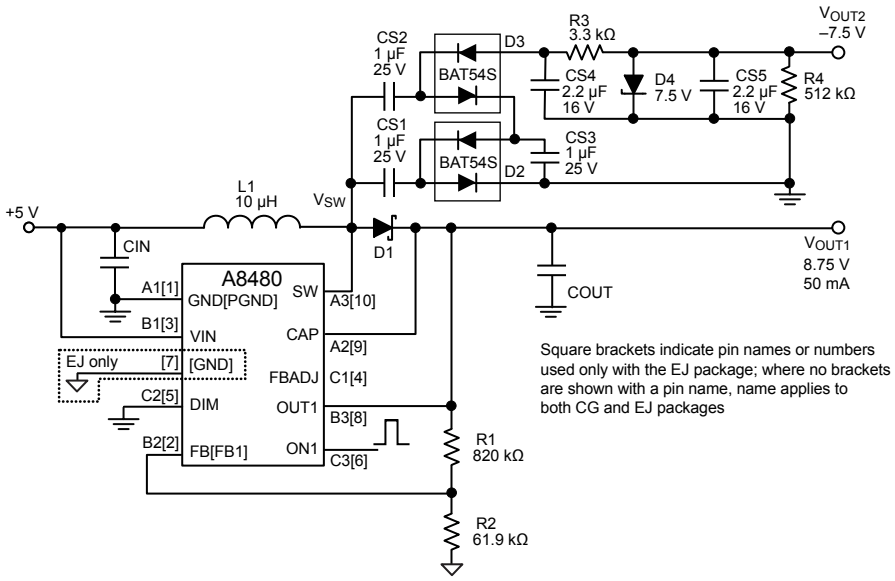


Figure 3a. Dual outputs (V_{OUT} and $-V_{OUT}$)

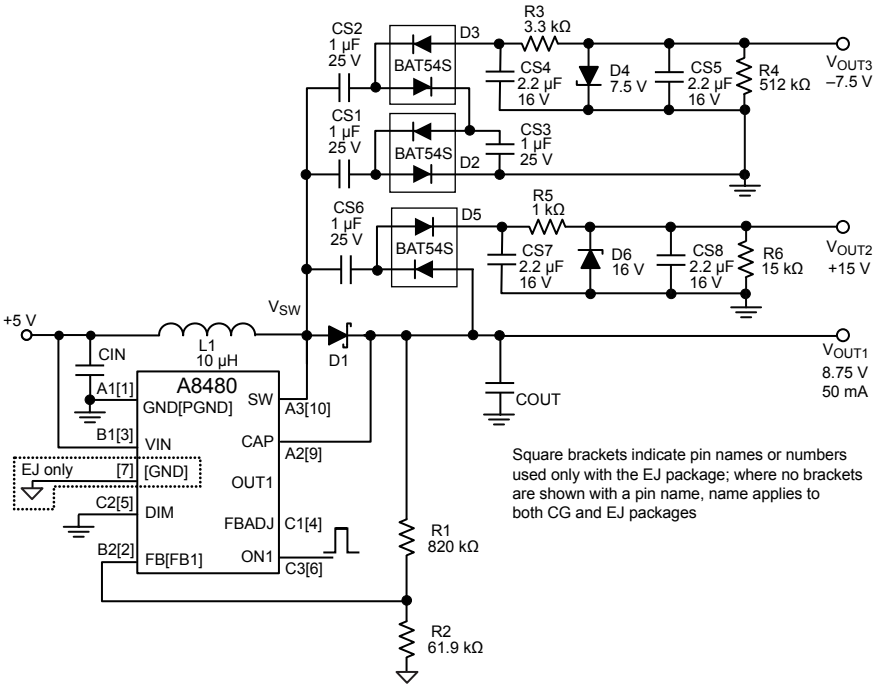
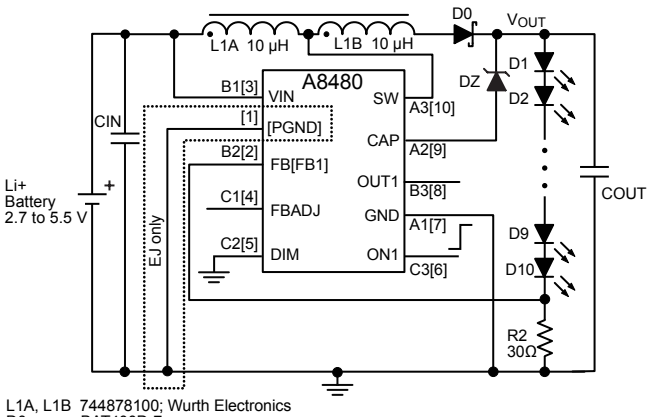
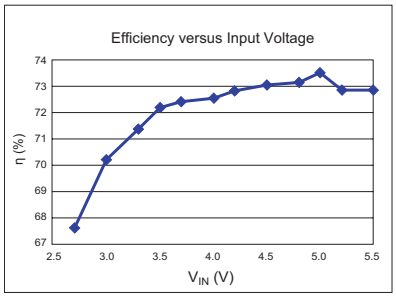


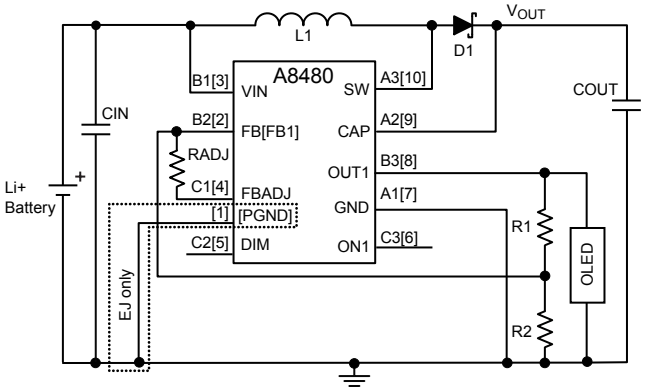
Figure 3b. Triple outputs (V_{OUT}, $-V_{OUT}$, and $2V_{OUT}$)





L1A, L1B 744878100; Wurth Electronics
D0 BAT400D-7
DZ IN4747ADICT
Square brackets indicate pin names or numbers used only with the EJ package;
where no brackets are shown with a pin name, name applies to both CG and EJ packages

Figure 4. Using the A8480 to drive 10 white LEDs (WLED)



Square brackets indicate pin names or numbers used only with the EJ package;
where no brackets are shown with a pin name, name applies to both CG and EJ packages

Figure 5a. Typical application circuit for A8480 driving an OLED with dimming.

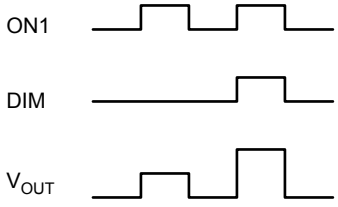
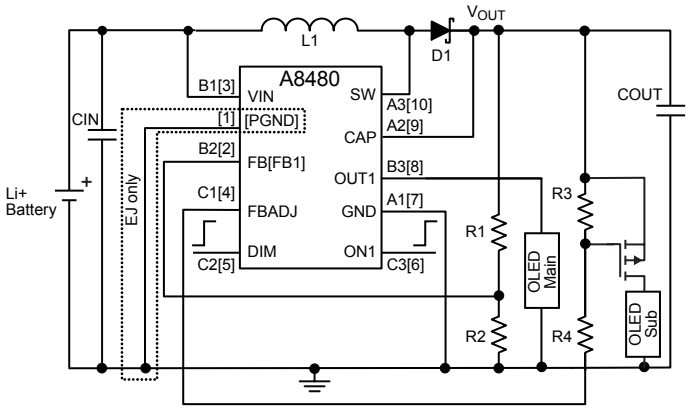
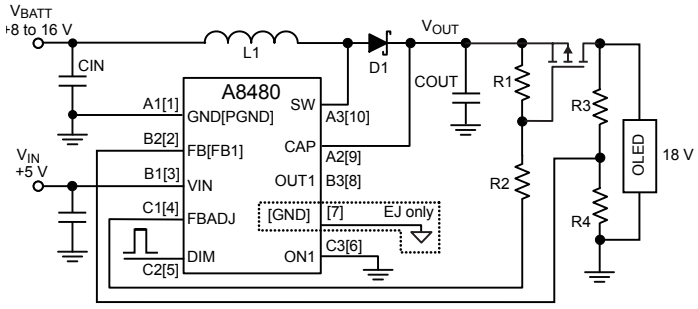


Figure 5b. Timing diagram for circuit shown in figure 5a.



Square brackets indicate pin names or numbers used only with the EJ package;
where no brackets are shown with a pin name, name applies to both CG and EJ packages

Figure 6. Main and sub OLED bias with both grounded



Square brackets indicate pin names or numbers used only with the EJ package;
where no brackets are shown with a pin name, name applies to both CG and EJ packages

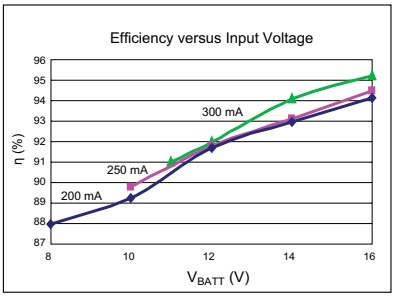
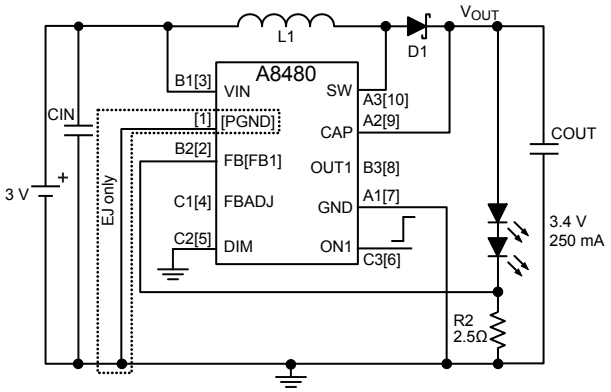
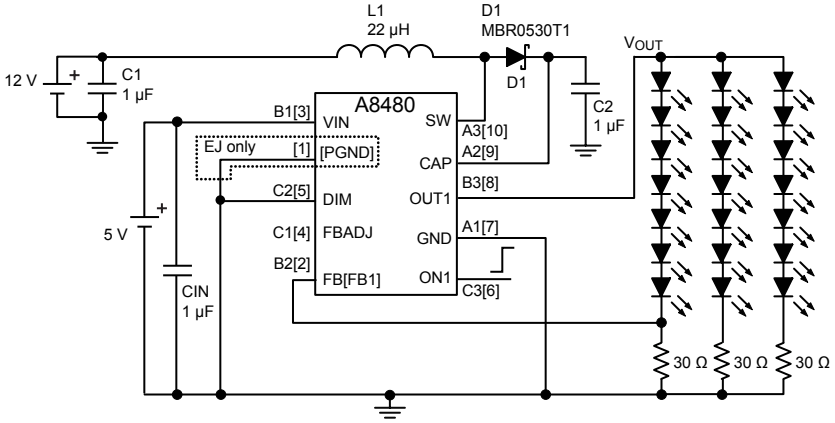


Figure 7. OLED supply for GPS/Auto Infotainment, with external output disconnect FET



Square brackets indicate pin names or numbers used only with the EJ package;
where no brackets are shown with a pin name, name applies to both CG and EJ packages

Figure 8. A8480 driving high current flash/torch LEDs

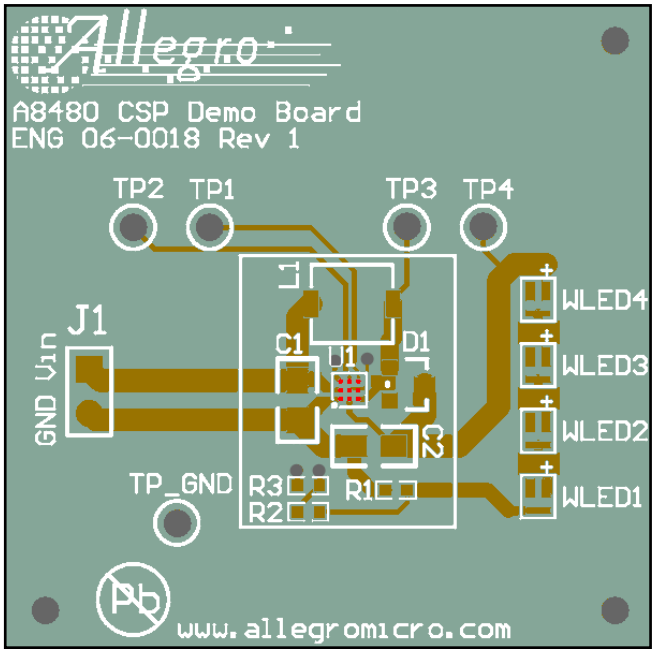


Square brackets indicate pin names or numbers used only with the EJ package;
where no brackets are shown with a pin name, name applies to both CG and EJ packages

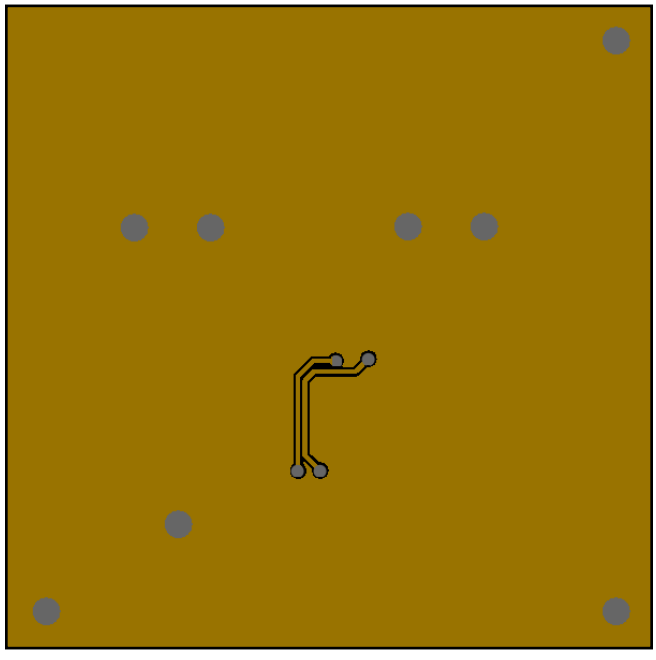
Figure 9. A8480 driving 21-LED frame for digital photograph display

Thermal Performance

The A8480 CSP package has low thermal impedance, $R_{\theta JA}$ = 109 °C/W.
This data was taken from tests performed on the CSP demonstration board.
The board layout is presented here for reference (enlarged for clarity).

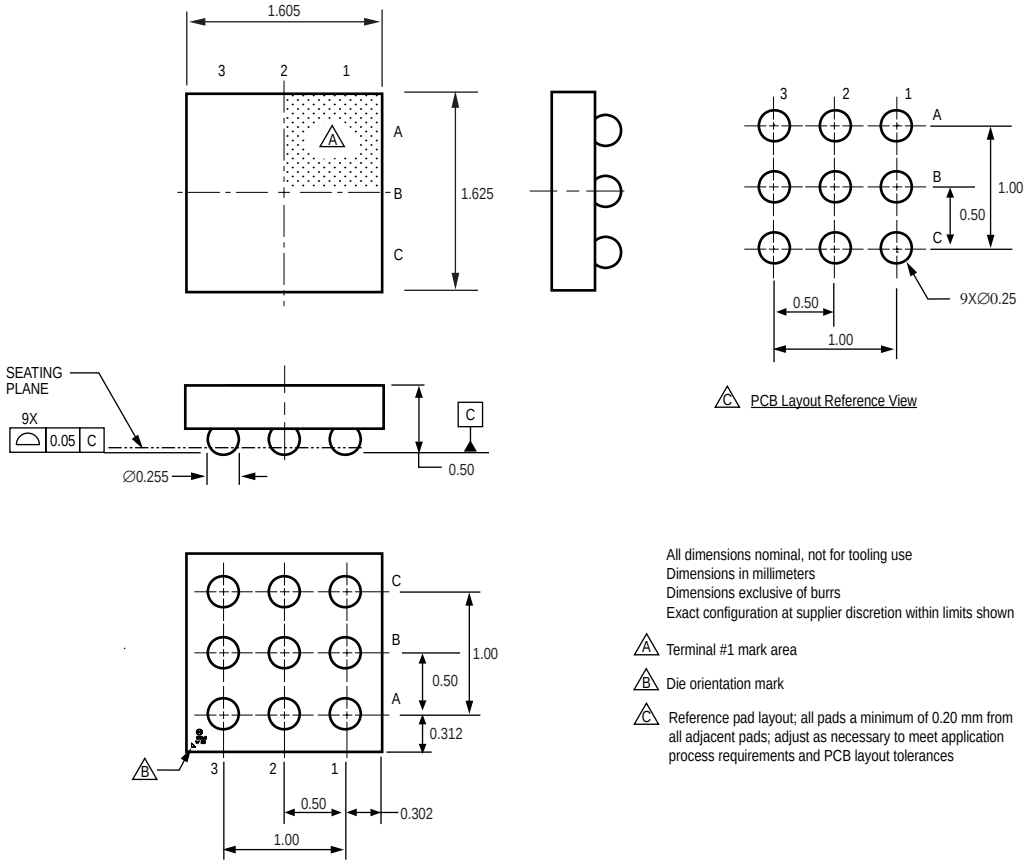


Top layer



Bottom layer

Package CG, 9-Pin CSP



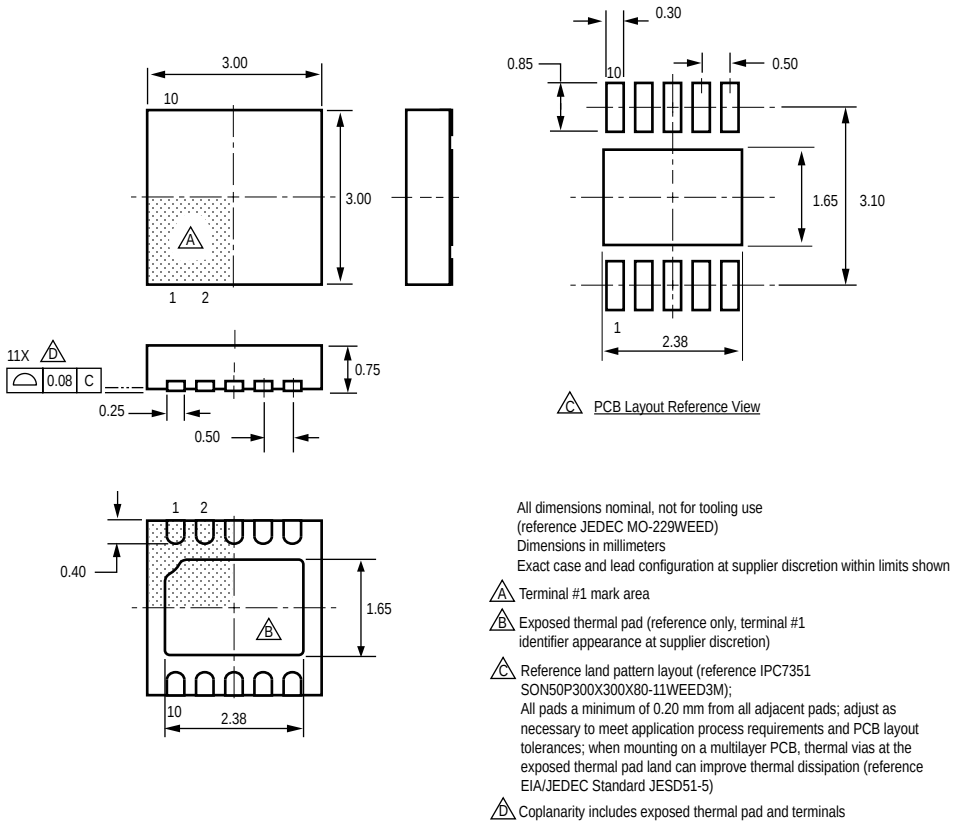
All dimensions nominal, not for tooling use
Dimensions in millimeters
Dimensions exclusive of burrs
Exact configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Die orientation mark

C Reference pad layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Package EJ, 10-Pin MLP/DFN



All dimensions nominal, not for tooling use
(reference JEDEC MO-229WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

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